memory cells on the die having a total combined area on the die which is no greater than 11 mm^2.

10. (Once amended) The semiconductor memory device of claim 6 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include at least five [composite] conductive line layers; the peripheral circuitry, the pitch circuitry and the memory arrays having a total combined continuous surface area on the die which is less than or equal to 32 mm^2.

18. (Twice amended) A 16M semiconductor memory device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of from 16,000,000 to 17,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die, at least one of the memory arrays containing at least <u>one area of</u> 100 square microns of continuous die surface area having at least 128 of the functional and operably addressable memory cells; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry,

and voltage supply circuitry which collectively enable full access to all addressable memory cells of the memory arrays.

19. (Once amended) The semiconductor memory device of claim 18 wherein at least one of the memory arrays containing at least one area of 100 square microns of continuous die surface area [having] has at least 170 of the functional and operably addressable memory cells.

22. (Once amended) A semiconductor memory device comprising:

a total of no more than 68,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on a semiconductor die; and

circuitry formed on the semiconductor die permitting data to be written to and read from one or more of the memory cells, at least one of the memory arrays containing at least one area of 100 square microns of continuous die surface area having at least 128 of the functional and operably addressable memory cells.

25. (Once amended) The semiconductor memory device of claim 22 wherein at least one of the memory arrays containing at least one area of 100 square microns of continuous die surface area [having]

has at least 170 of the functional and operably addressable memory cells.

26. (Once amended) The semiconductor memory device of claim 22 wherein at least one of the memory arrays containing at least one area of 100 square microns of continuous die surface area [having] has at least 170 of the functional and operably addressable memory cells, and the total number of functional and operably addressable memory cells on the semiconductor die is no more than 17,000,000.